Remarks/Arguments

In the Office Action mailed on April 20, 2007, the Examiner rejected claims 1-6, 8-22 and 24-25 under 35 U.S.C. §103(a) as unpatentable over Shinozaki (U.S. Patent No. 6,333,875) in view of Crafts (U.S. Patent No. 5,231,319).

Applicants respectfully traverse the rejection and request reconsideration and withdrawal of same.

35 U.S.C. §103(a) Rejection

The Examiner rejected claims 1-6, 8-22 and 24-25 under 35 U.S.C. §103(a) as unpatentable over Shinozaki in view of Crafts. Applicants respectfully traverse the rejection, as the combination of Shinozaki and Crafts, or any of the prior art or record considered individually or in any combination, does not teach or reasonably suggest the systems and methods recited by the claims of the present application. The rejection will be discussed in regard to independent claim 1.

Claim 1 is directed at a system for latching data. Present day circuits have overhead delays caused by fabrication process variations and operating conditions of the circuit. These overhead delays may vary across the surface of the circuit, leading to varying delays at different physical locations of the integrated circuit die. Thus, a delayed signal generated at one physical location of the circuit with a particular designed delay value may be additionally delayed due to local overhead variations in comparison with similarly delayed signals generated elsewhere on the circuit designed with the same delay value. The local overhead variation adds additional delay to the designed delay, causing the actual delay to be higher than the designed delay. As circuit speeds have increased, this overhead delay has become a measurable portion of the intended programmed delays. Thus, the overhead delay may cause timing errors such as when clocking data signals. Therefore, a data signal and a strobe signal may not be properly aligned, and data corruption may occur.

The system of amended claim 1 solves this problem by providing a first delay circuit configured for programmably delaying a strobe signal with a first delay to latch an associated data signal. The first delay circuit has an overhead delay that varies based on fabrication process variations or operating conditions of the first delay circuit. As a

result, the overhead delay effectively adds to the programmed first delay by the amount of time of the overhead delay. A second delay circuit in close proximity to the first delay circuit delays the data signal with a second delay. Because the second delay circuit is in close proximity to the first delay circuit, the second delay circuit has substantially identical fabrication process variations and/or operating conditions as the first delay circuit. These identical process variations and operating conditions generate substantially the same overhead delay in the first and second delay circuits. The second delay is then substantially identical to the overhead delay of the first circuit. Thus, the second delay circuit is able to effectively compensate for the associated overhead delay from the first delay so that the strobe signal and data signal are properly aligned.

By contrast, Shinozaki discloses a semiconductor circuit which receives a strobe signal and a data signal. The circuit includes a latch-signal-generation circuit which generates a first latch signal delay by a first delay time relative to the strobe signal and a second latch signal inverted and delayed by a second delay time relative to the strobe signal. A control circuit adaptively controls the latch-signal-generation circuit to adjust timings of the first and second latch signals such that the first delay time and the second delay time become substantially equal. The data signal is then latched at edge timings of the first and second latch signals. Thus, the latch signals are created with delays substantially equal for latching a data signal at rising and falling edges of a clock signal (Abstract of Shinozaki).

Crafts discloses a circuit having two similarly fabricated series arranged inverter elements placed in parallel. One of the series arranged inverters is used as an operating circuit (i.e., for carrying a strobe signal), while the other of the series arranged inverters is used as a reference circuit (Abstract of Crafts). Particularly, a delay circuit 10A of Crafts applies an actual delay to a signal before the signal emerges at the output of delay circuit 10B (col. 5, lines 54-55 of Crafts). A delay circuit 10B has the same signal applied to its input, and provides a measurement signal at its output stage which measures the delay applied by delay circuit 10A (col. 5, lines 56-58 of Crafts). Delay circuit 10B can track the delay imparted by circuit 10B, because the two variable delay circuits 10A and 10B are fabricated or formed in close proximity on the integrated circuit chip so that the temperature, voltage and process variables that affect their delay times will closely track

each other (col. 5, lines 58-62 of Crafts). A comparator 56 then compares the output of delay circuit 10B to determine whether delay circuit 10A has applied the desired delay to the input signal. If delay circuit 10A has not applied the desired delay, then the voltage of the reference control signal applied to delay circuit 10A can be adjusted until the desired delay is applied by delay circuit 10A to the input signal (col. 6, lines 5-33 of Crafts). In essence, the illustrated circuit of Crafts in FIG. 5 measures and adjusts the time delay of delay circuit 10B (the reference circuit) so as to control and adjust the time delay of delay circuit 10A (the operating circuit).

At least one feature of claim 1 not taught or reasonably suggested by the combination of Shinozaki and Crafts, or any of the prior art of record, considered individually or in any combination is a second delay circuit configured for delaying a data signal with a second delay that is substantially identical to the overhead delay of a first delay circuit (delaying a strobe signal) to compensate for overhead delay associated with the first delay. The Examiner states that Shinozaki teaches a delay circuit 28 which is equivalent to the second delay circuit recited by claim 1. Applicants respectfully disagree.

Neither Shinozaki nor Crafts teach delaying a data signal by a delay that is substantially identical to the overhead delay of a first delay circuit delaying a strobe signal. The Examiner asserts that col. 1, lines 54-65 of Shinozaki teaches this recited feature. Shinozaki teaches a system that generates two latch signals SA and SB from a signal strobe signal DSQ, with SB being inverted in comparison to SA (col. 1, lines 26-30 of Shinozaki). The passage cited by the Examiner (i.e., col. 1, lines 54-65 of Shinozaki) discloses that control circuitry can be utilized to adjust the timing of the delays used to generate the two latch signals such that the first delay time and the second delay time of each latch signal is substantially equal.

Specifically, Shinozaki discloses creating adjustable delays *ta* and *tb* applied to two different latch signals, such that the difference between the two delays is substantially zero (e.g., within a specific tolerance) (Shinozaki, col. 4, lines 8-21). If the difference between delays *ta* and *tb* is not zero, then a programmable delay is used to adjust the difference between the latch signals. Thus, Shinozaki uses a feedback loop and

several programmable delays to equalize the difference between the two delays, allowing multiple latch signals to be aligned with rising and falling edges of the strobe signal.

Thus, the substantially identical delays generated by Shinozaki are applied to latch signals and not data signals. By contrast, the second delay circuit of claim 1 applies a delay to the data signal that is substantially identical to the overhead delay of the first delay circuit to compensate for the overhead delay applied to the strobe signal by the first delay circuitry. Shinozaki does not teach or reasonably suggest equalizing delays applied to both a data signal and a strobe signal in order to compensate for overhead delays of one or more of the delay circuits applying delays to both signals.

Crafts does not alleviate the deficiencies of Shinozaki, because Crafts uses a similar structure to Shinozaki to measure and adjust a delay applied by a single delay circuit to an input signal. Specifically, Crafts teaches utilizing two delay circuits 10A and 10B, one delay circuit 10A applying a delay to actual data intended as output, and the other delay circuit 10B applying a delay to data used for measurement purposes only and not as output (see col. 5, lines 51-57 of Crafts). If the desired delay measured on the measurement circuit 10B is not a desired delay applied by delay circuit 10A applying a delay to the actual output data, then the applied delay of both delay circuits 10A and 10B can be adjusted so that the desired delay is applied to the actual data signal. There is no suggestion or motivation (let alone actual teaching) that the measurement and adjustment done by delay circuits 10A and 10B is utilized to equalize the overhead delay of a data signal and a strobe signal. Thus, Applicants submit that the combination of Shinozaki and Crafts, or any of the prior art of record considered individually or in any combination, does not teach the second delay circuit of claim 1.

Further, Applicants submit that the combination of Shinozaki and Crafts does not teach or reasonably suggest placing a first delay circuit applying a delay to a data signal in close proximity to a second delay circuit applying a delay to a strobe signal such that both signals have the same inherent overhead delay. Rather, as discussed above, Crafts teaches placing two delay circuits 10A and 10B (delaying the same input data signal) in close proximity so that one of the outputs from delay circuit 10B can be used to measure the delay applied to the data signal by the other delay circuit 10A. The two delay circuits 10A and 10B are in close proximity for measurement purposes only, and not in close

proximity for applying a similar overhead delay to multiple distinct input signals (i.e., a strobe and a data signal). Thus, Applicants submit that the combination of Shinozaki and Crafts, or any of the prior art of record considered individually or in any combination, does not teach the close proximity feature of claim 1.

Further, Applicants submit that Shinozaki and Crafts both use comparison logic circuits to make adjustments to delays applied to signals. Particularly, Shinozaki utilizes comparison circuit 74 (see FIG. 3) to dynamically adjust the delays applied to SA and SB such that they are substantially equal delays (col. 6, lines 44-52 of Shinozaki). Likewise, Crafts uses comparator 56 to determine whether adjustments are needed to the delay applied by delay circuit 10A (see col. 6, lines 5-20). By contrast, the system of claim 1 does not utilize active comparison logic to equalize delays between the strobe signal and the data signal. Rather, the system of claim 1 passively equalizes the overhead delay between the strobe signal and the data signal by placing both delay circuits in close proximity so that both delay circuits have the same inherent overhead delay. Applicants submit that this feature of claim 1 is not taught or reasonably suggested by Shinozaki and Crafts, or any of the prior art of record considered individually or in any combination.

In view of the above discussion, Applicants maintain that independent claim 1 is distinguished over the teachings of the combination of Shinozaki and Crafts. The claims are neither taught nor reasonably suggested by the combination of Shinozaki and Crafts, or by any art of record, considered individually or in any combination. Applicants maintain that independent claims 8, 13 and 18 are distinguished for at least the same reasons discussed above.

Dependent claims 2-6, 9-12, 14-17, 19-22 and 24-25 are allowable for at least the same reasons and as dependent upon allowable base claims. Additionally, dependent claims 2-6, 9-12, 14-17, 19-22 and 24-25 recite additional limitations not found in the prior art of record. Applicants respectfully request reconsideration and withdrawal of the outstanding rejection of claims 1-6, 8-22 and 24-25.

Conclusion

The Examiner's rejection of claims 1-6, 8-22 and 24-25 has been thoroughly discussed. Applicants request reconsideration and withdrawal of the outstanding rejection and allowance of claims 1-6, 8-22 and 24-25.

Applicants believe that no fees are due in this matter. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

Respectfully submitted,

Date: July 20, 2007

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